Contact Information

- Instructor: Dr. Gregory Wolffe  (wolffe@gvsu.edu)
- Office:  718 Eberhard Center (331-6824)
- Hours:  Monday, Wednesday  5:00 - 6:00,  and whenever.
- Info Page:  http://www.cis.gvsu.edu/~wolffe/courses/cs459
  Includes all course policies, announcements, assignments and class documents.

Course Description and Objectives

Design issues and software engineering methodologies for embedded computer systems development.
To obtain a working knowledge of programming techniques for a real-time embedded microprocessor.
Topics covered include:

- CPUs and instruction sets
- Processes, threads, and scheduling
- Memory, I/O devices, and interconnects
- Program and system design
- Efficient and optimized coding

Suggested Prerequisites

- Hardware background: EGR 226 or CS 251
- Software background: EGR 261 or CS 361

Textbooks

Required:

- Computers as Components;  Wayne Wolf; Morgan Kaufmann; 2001.

Grading

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<thead>
<tr>
<th>Grading</th>
<th>Grading Scale</th>
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<tbody>
<tr>
<td>20% Homework</td>
<td>A  90%</td>
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<tr>
<td>40% Lab assignments</td>
<td>B  80%</td>
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<tr>
<td>40% Exams</td>
<td>C  70%</td>
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<td>D  60%</td>
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<td>F  &lt;60%</td>
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Course Policies

- Homework and programming projects are due at the beginning of class on the due date.  NO late
  assignments will be accepted unless prior arrangements have been made.
- Homework assignments, unless otherwise specified by the instructor, are to be completed
  individually. Students are encouraged to consult each other for instructional assistance only.
- Exams may only be rescheduled with prior approval of the instructor.
- The deadline to drop with a “W” is Tuesday, June 9th, at 5:00 p.m.
Course Outline

1. Introduction / Background

2. Design
   • Modeling and analysis
   • Specification and Design
   • Programming techniques
   • Design methodologies

3. Instruction Sets
   • Data processing
   • Control transfer
   • Memory access

4. CPUs
   • Registers
   • Pipelining
   • Interrupts, exceptions
   • Performance evaluation

4. Scheduling
   • Processes
   • Threads
   • Scheduling policies
   • Synchronization and concurrency

5. Memory
   • Memory management unit
   • Protected memory
   • Cache memory

6. Computing Platform
   • I/O devices
   • Interconnects
   • Networking
   • Data communications

Midterm: Wednesday, 5/24
Final Exam: Wednesday, 6/21 (6:00 - 7:50 p.m.)